IN THE CLAIMS:

Kindly **amend** the claims as follows:

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151. (Amended) A method of controlling [operating] a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of controlling the memory device comprises [comprising]:

providing first block size information to the memory device, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read [or write] request; and

issuing a first read request to the memory device, wherein in response to the first read request, the memory device outputs the first amount of data corresponding to the first block size information onto the bus synchronously with respect to an external clock signal.

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152. (Amended) The method of claim 151 wherein first block size information further defines a first amount of data to be input by the memory device from the bus in response to a write request, the method further including [providing] issuing a first write request to the memory device wherein, in response to the first write request, the memory device inputs the first amount of data corresponding to the first block size information from the bus synchronously with respect to the external clock signal.

153. (Amended) The method of claim 152 further including:

providing second block size information to the memory device, wherein the second block size information defines a second amount of data to be input by the memory device from the bus in response to a write request; and

issuing the second write request to the memory device, wherein in response to the second write request, the memory device inputs the amount of data corresponding to the second block size information from the bus synchronously with respect to the external clock signal.

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168. (Amended) A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells, the method of operation of the memory device comprises [comprising]:

receiving an external clock signal;

receiving first block size information from a bus controller, wherein the first block size information defines a first amount of data to be output by the memory device onto a bus in response to a read [or write] request;

receiving a first read request from the bus controller; and

outputting the first amount of data corresponding to the first block size information, in response to the first read request, onto the bus synchronously with respect to [an] the external clock signal.

169. (Amended) The method of claim 168 further including:

receiving a second read request from the bus controller, and

outputting the first amount of data corresponding to the first block size information, in response to the second read request, onto the bus synchronously with respect to the external clock signal.

170. (Amended) The method of claim 168 wherein first block size information further defines a first amount of data to be input by the memory device from the bus in response to a write request, the method further including:

receiving a first write request from the bus controller, and

inputting the first amount of data corresponding to the first block size information, in response to the first write request, from the bus synchronously with respect to the external clock signal.

171. (Amended) The method of claim 170 further including:

receiving second block size information, wherein the second block size information defines a second amount of data to be input from the bus in response to a write request; and

receiving the second write request from the bus controller;

inputting the amount of data corresponding to the second block size information, in response to the second write request, from the bus synchronously with respect to the external clock signal.

184. (Amended) A method of operation of a synchronous memory device, wherein the memory device includes a plurality of memory cells and a time delay register, the method of operation of the memory device comprises:

storing a value in the time delay register, the value being representative of a number of external clock cycles to transpire after which the memory device responds to a read request;

receiving an external clock signal wherein the external clock signal has a fixed frequency;

receiving block size information from a bus controller, wherein the block size information defines a first amount of data to be output by the memory device onto the bus in response to a read request;

receiving a first read request from the bus controller;

outputting the first amount of data corresponding to the block size information onto the bus in response to the first read request.[;

receiving a second read request;

outputting the first amount of data corresponding to the block size information onto the bus in response to the second read request; and]

wherein the memory device outputs the data synchronously with respect to the external clock signal, during a plurality of clock cycles of the external clock signal and in accordance with the value stored in the time delay register.